



IDS Form PTO/SB/08: Substitute for form 1449A/PTO

Complete if Known

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/086,544
		Filing Date	3/4/02
		First Named Inventor	YUTAKA ARIMA
		Art Unit	2121
		Examiner Name	Joseph P. H...
Sheet 1 of 1	Attorney Docket Number	08372-0007	Group 2100

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS					
Examiner Initials	Cite No. ¹	Document Number	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

Note: Copies of the U.S. Patent Documents are not Required in IDS filed after October 21, 2004

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation ⁶
H		YUTAKA ARIMA, "Higher Integration of Neural Network with Learning Function," Study of Associative Memory Analog Neural Network LSI with Learning Function (January 1998).	✓
H		"Chaos and Associative Memory," Computer Today (July 1999).	✓
H		YUTAKA ARIMA, et al., "A Self Learning Neural Network Chip with 125 Neurons and 10K Self-Organization Synapses," 26 IEEE Journal of Solid-State Circuits 607 (April 1991).	
H		YUTAKA ARIMA, et al., "A 336-Neuron, 28K-Synapse, Self-Learning Neural Network Chip with Branch-Neuron-Unit Architecture," 26 IEEE Journal of Solid-State Circuits 1637 (November 1991).	
H		YUTAKA ARIMA, et al., "A Refreshable Analog VLSI Neural Network Chip with 400 Neurons and 40K Synapses," 27 IEEE Journal of Solid-State Circuits 1854 (December 1992).	

Examiner Signature		Date Considered	1/13/05
--------------------	---	-----------------	---------

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PTO Notes regarding this form:

- ¹ Applicant's unique citation designation number (optional).
 - ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.
 - ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).
 - ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.
 - ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.
 - ⁶ Applicant is to place a check mark here if English language Translation is attached.
- This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**